REMARKS

Claims 1-25 are presented for examination.

Claims 1 and 13 have been objected to. In response, the word "maximum" has been deleted per the Examiner's request.

REJECTIONS UNDER 35 U.S.C. 112

Claims 1-25 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Regarding claim 1, this claim, as amended, recites *inter alia* the steps of determining whether a pre-determined decoder termination threshold metric has been met; and identifying frames for use in further processing after a pre-determined number of decoder iterations.

The Examiner requested claim 1 to recite determining whether a pre-determined decoder termination threshold metric has been met but only after a predetermined number of decoder iterations, and identifying frames for use in further processing.

As explained in more detail below, the "pre-determined decoder termination threshold metric" is not the same as the "pre-determined number of decoder iterations". Therefore, changing the claim language in accordance with the Examiner's request would make the claims inconsistent with the present invention.

Regarding claim 13, the Examiner takes the position that the specification does not support separate threshold metric processor for determining whether a pre-determined decoder termination threshold metric has been met, and maximum iteration processor for identifying frames for use in further processing.

This position is respectfully traversed. The Examiner's attention is directed to page 7, lines 7-13 of the specification and figure 5, which clearly describe and illustrate threshold metric

processor 502 and maximum iteration processor 512. Although the description states that the threshold metric processor comprises a maximum iteration processor, these processors perform different functions and for clarity have been detailed in the claims as separate processors.

To assist Examiner in understanding the present invention, the Applicant provides the following brief description of the invention defined in claims 1 and 13.

The apparatus/method of the invention aims to successfully decode data. The data is turbo decoded. After each decoding, it is determined whether the data has been decoded a pre-set number of times (for example 5 times). If the data has been decoded the pre-set number of times (i.e. the threshold metric has been met), then the data is subject to a cyclic redundancy check (CRC) test. If the CRC test determines that the data has been successfully decoded, then the apparatus/method stops. However, if the CRC test determines that the data has NOT been successfully decoded, then the apparatus/method returns the data to the turbo decoder for further decoding.

The apparatus/method of the invention also includes a maximum iteration processor (which was added to the claims following the previous office action). The maximum iteration processor determines which data has passed the threshold metric test and the CRC test, but only after a pre-set number of iterations (the pre-determined number of decoder iterations), and marks this data for further processing.

Thus, any data which has been turbo decoded the pre-set number of times; CRC tested; returned to the turbo decoder and decoded the pre-set number of times; CRC tested; returned to the turbo decoder and decoded the pre-set number of times, etc,...until the CRC test determines that the data has been decoded, are marked for further processing when the total number of turbo

decoding iterations is greater than a pre-set maximum number of iterations (the pre-determined number of decoder iterations).

For example, the data may be turbo decoded 5 times before it is passed for a CRC test. Thus the threshold metric c is 5. However, the data may have been turbo decoded a total of 20 times before the CRC test is passed, i.e. the data has been subjected to four lots of 5 turbo decoding. If the pre-determined number of decoder iterations is set as 20, this data would then be marked for further processing. This is because, since the decoding involved many turbo decoding and CRC checks the decoded frame of data is considered to be suspect (it may not have been properly decoded even though the CRC test is passed). Therefore, the apparatus/method marks this frame of "decoded" data for further processing.

It is believed that claims 1 and 13, as now amended, fully comply with the statutory requirement to set out and circumscribe a subject matter area with a reasonable degree of precision and particularity.

REJECTION UNDER 35 U.S.C. 102

Claims 1, 6-11, 13, 18-23 and 25 stand rejected under 35 U.S.C. 102(b) as being anticipated by Sindhushayana (US patent 6,292,918).

The Examiner's rejection is respectfully traversed for the following reasons.

Claim 1 recites a method for decoding a received sequence of symbols of a frame using a turbo decoding process that comprises a plurality of decoder iterations. the method comprises:

-determining whether a pre-determined decoder termination threshold metric has been met;

-identifying frames for use in further processing after a pre-determined number of decoder iterations;

-only if the threshold metric has been met, determining whether a decoder termination test based on a cyclic redundancy check code has been passed; and

-only if the cyclic redundancy check test has been passed, terminating the decoder iterations.

Independent claim 13 recites an apparatus for decoding a received sequence of symbols of a frame using a turbo decoding process that comprises a plurality of decoder iterations. The apparatus comprises:

-a threshold metric processor for determining whether a pre-determined decoder termination threshold metric has been met;

-a maximum iteration processor for identifying frames for use in further processing after a pre-determined number of decoder iterations;

-a cyclic redundancy check processor for determining, only if the threshold metric processor determines that the threshold metric has been met, whether a decoder termination test based on a cyclic redundancy check code has been passed; and

-a decoder termination means for terminating the decoder iterations, only if the cyclic redundancy check test has been passed.

It is respectfully submitted that the reference does not disclose the step of identifying frames for use in further processing after a pre-determined number of decoder iterations, as claim 1 recites.

Also, the reference does not disclose a maximum iteration processor for identifying frames for use in further processing after a pre-determined number of decoder iterations, as recited in independent claim 13.

Instead of identifying frames for use in further processing after a pre-determined number of decoder iterations, Sindhushayana discloses that iteration would continue until the CRC test is passed. However, even if the CRC test is passed there may still be an error in the received symbols, and these received symbols are not identified or marked for further processing.

It is noted that the Examiner has failed to point out specifically wherein Sindhushayana discloses the claimed maximum iteration processor for identifying frames for use in further processing after a pre-determined number of decoder iterations, or the respective claimed step.

Instead, The Examiner indicates that the reference discloses determining absolute probability value and concludes that thereby Sindhushayana discloses determining whether a pre-determined decoder termination threshold metric has been met after a pre-determined number of decoder iterations.

However, the claims recite "identifying frames for use in further processing after a pre-determined number of decoder iterations."

Hence, the Examiner's conclusion of anticipation is unwarranted.

REJECTION UNDER 35 U.S.C. 103

Claims 2-5, 12, 14-17, and 24 have been rejected under 35 U.S.C. 103 as being unpatentable over Sindhushayana.

It is respectfully submitted that the Examiner's statement that Applicant does not disagree with the Examiner's characterization of the claims as being "well known" is inaccurate.

In the previous response, Applicant demonstrated that the Examiner has failed to establish a **prima facie** case of obviousness by failing to provide an obviousness analysis in connection with claims 2-5, 12, 14-17, and 24.

It is well settled that the Examiner bears the initial burden of establishing a ***prima facie*** basis to deny patentability to a claimed invention under any statutory provision. ***In re Oetiker***, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). It is respectfully submitted that the Examiner did not discharge that burden.

Recent decisions of the USPTO Board of Appeal and Interferences in ***Ex parte Smith,*** Appeal 2007-1925 (June 25, 2007) and ***Ex parte Catan,*** Appeal 2007-0820 (July 3, 2007) that follow the Supreme Court's decision in ***KSP Int'l Co. v. Teleflex Inc.,*** 127 S.Ct. 17127 (2007) put forth an obviousness analysis that emphasizes a functional approach based on ***Graham v. John Deere*** factors. As stated in ***Graham v. John Deere Co.*** 383 U.S. 1, 13, 148 U.S.P.Q. 459, 465 (1966), obviousness under 35 U.S.C. §103 must be determined by (1) analyzing the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; (3) resolving the level of ordinary skill in the pertinent art, and (4) analyzing secondary considerations.

As the Examiner admits, the prior art differs from the claimed subject matter. Accordingly, an obviousness analysis based on ***Graham v. John Deere*** factors indicates that the claims are not obvious over the prior art.

The Examiner's position that the differences are "well known" is respectfully traversed. For example, the dependent claims 2-5 and 14-17 recite elements of the claimed threshold metric processor or operations for determining whether the threshold metric has been met. The Examiner has failed to provide a basis in fact and/or cogent technical reasoning to support his conclusion that the claimed elements of the threshold metric processor or operations for determining whether the threshold metric has been met are well known in the art.

In the previous response, Applicant requested the Examiner to cite a reference in support of his position in accordance with MPEP 2144.03. However, the Examiner did not address this request.

Accordingly, Applicant respectfully submits that the rejections of claims 2-5, 12, 14-17, and 24 under 35 U.S.C. 103 as being unpatentable over Sindhushayana is improper because the Examiner has failed to establish a **prima facie** case of obviousness.

In view of the foregoing, and in summary, claims 1-25 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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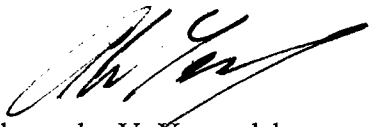

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